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APPLICATION FOR LETTERS PATENT

for

**SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION CIRCUITRY
FOR COMPRESSING TEST DATA, AND THE TEST SYSTEM AND METHOD FOR
UTILIZING THE SEMICONDUCTOR INTEGRATED CIRCUIT**

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**SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION
CIRCUITRY FOR COMPRESSING TEST DATA, AND THE
TEST SYSTEM AND METHOD FOR UTILIZING THE
SEMICONDUCTOR INTEGRATED CIRCUIT**

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Serial No. 09/175,518, filed October 20, 1998, pending, which is a continuation of application Serial No. 08/881,946, filed June 25, 1997, now U.S. Patent 5,864,565, issued January 26, 1999, which is a continuation of application Serial No. 08/353,404, filed Dec. 9, 1994, now abandoned, which is a continuation-in-part of application Serial No. 08/077,182, filed June 15, 1993, now abandoned.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The invention relates to semiconductor integrated circuits and, more particularly, to internal test circuitry of a semiconductor integrated circuit.

[0003] Background of the Invention: Semiconductor integrated circuits are typically tested in response to an applied input test signal. The semiconductor integrated circuits respond to the input test signal by providing a test output signal which is monitored to determine if the part has been manufactured correctly. With an increase in storage capacity and memory circuit functions, the testing of a semiconductor integrated circuit consumes more time and requires more testing hardware.

[0004] In Figure 1, a memory component tester 5 of the related art is shown which has 4 test stations 7-10. Each test station 7-10 is used to test circuit functions of an individual semiconductor integrated circuit or, during testing known as, a device under test (DUT). Therefore when testing, say, four integrated circuits 12-15, as shown in Figure 1, four test stations 7-10 are needed. Typically, each test station 7-10 has a number of pins 20 corresponding to the number of I/O (input/output) pins 25 on the DUT for coupling the test station to the DUT during testing. The DUT responds to applied test signals originating in the memory component tester 5 and generates test output signals in response to the applied test signals. The test stations monitor the test output signals to determine if a DUT has been manufactured correctly.

[0005] The ability to test in parallel is limited by the number of Pin Electronic Channels with comparator capability a memory component tester may have. How those limited resources are utilized by the product tested on test equipment is directly related to designing a test mode which makes best use of each Pin Electronics Channel. The present Micron Test Mode tri-states each unique I/O pin individually upon failure. This prevents the tying of multiple I/O pins together for greater parallel testing because a failing pin in a high impedance state is driven by a passing pin to a passing voltage level. The driving pin (Passing) would mask the tri-stated (failing) pin which would cause the failure to go undetected, and the failed part would be binned with those which passed testing.

[0006] In order to reduce the total manufacture time and decrease manufacturing costs there is a need to develop a faster testing method requiring less test equipment.

SUMMARY OF THE INVENTION

[0007] The invention is a semiconductor integrated circuit, method and test system for compressing test stimuli to one test output signal during a test mode. The test output signal is driven from one input/output node of the semiconductor integrated circuit to a test station through a load board interface of the invention. Buffer circuitry on the semiconductor integrated circuit drive a high impedance to the input/output nodes of the integrated circuit during the test mode. The load board interface allows a single test station to receive test output signals from a plurality of semiconductor integrated circuits of the invention during the test mode, thereby allowing one test station to simultaneously test a plurality of circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a block schematic of integrated circuits and a memory component tester of the related art.

[0009] Figure 2 is a block schematic of the semiconductor integrated circuit and a load board of the invention and a memory component tester.

[0010] Figure 3 is a simplified block schematic of the load board of Figure 2.

[0011] Figure 4 is a schematic of the buffer bank shown in the block schematic of Figure 2.

[0012] Figure 5 is a schematic of the comparator circuit shown in the block schematic of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Figure 2 is a block schematic of a semiconductor integrated circuit 50 of one embodiment of the invention. The semiconductor integrated circuit 50 comprises memory and peripheral circuitry 55 for memory storage and retrieval in a user environment. During a test mode, typically performed subsequent to encapsulation of the semiconductor integrated circuit 50, input test data supplied by a test station 60 of a memory component tester 65 is applied on input/output (I/O) pins 70 having designations A-D. Designations A-D are used throughout this description to identify corresponding pins or nodes. A load board interface 75 of the invention couples the integrated circuit 50 to the test station 60. An output enable signal at node 76 controls an input/output buffer 80 to couple the input test data on input/output pins 70 to demux output nodes 85 during a test mode. The demux output nodes 85 are connected to input nodes 90 of the memory and peripheral circuitry 55. During normal operation the semiconductor integrated circuit 50 is disconnected from the load board interface 75 and input data is coupled from input/output pins 70 and input nodes 90 through the input/output buffer 80 in response to the output enable signal at node 76.

[0014] The memory and peripheral circuitry 55 respond to the input test data to provide output test data internally at nodes 95, which are input nodes to a test data comparator circuit 100 of the invention and a buffer enable bank 105 of the invention. The test data comparator circuit 100 compares the output test data at nodes 95 and provides a test output signal at comparator output node 110 when enabled by a test mode enable signal having a first logic state at test mode node 118. Therefore, the output test data at nodes 95 are compressed into one test output signal which indicates a pass or fail of the semiconductor integrated circuit 50. The comparator output node 110 is connected to one of the output nodes 119 of buffer enable bank 105, in this case D. The potential of the test output signal at comparator output node 110 has a first or second logic

state, typically a high or a low, when all of the output test data at nodes 95 have a same logic state and a high impedance appears at comparator output node 110 when there is a difference in logic states of the output test data at nodes 95. When all of the output test data is the same, the memory and peripheral circuitry 55 is responding correctly to the input test data at nodes 90, and when at least two of the output test data have different logic states, the memory and peripheral circuitry 55 is not responding correctly to the input test data at nodes 90.

[0015] The buffer enable bank 105, with internal blocks A-D, drives a potential or presents a high impedance to nodes 119 as directed by the testmode signal at node 76. During a first test mode, a high impedance state is present on nodes 119, regardless of the value of the output test data at nodes 95, unless the high impedance is overridden by another signal such as the test output signal. Since the buffer enable bank 105 has driven node 119-D to a high impedance state during the first test mode, the test output signal on comparator output node 110 drives the potential of node 119-D to either a high or low logic state when the test data output at nodes 95 have a same logic state, and the high impedance state remains on node 119-D when there is a difference in the logic states of the output test data at nodes 95.

[0016] The load board interface 75 provides an electrical interface between four semiconductor integrated circuits 50 and 115-117 of the invention and four input/output (I/O) pins 120 of test station 60. Semiconductor integrated circuits 115-117 have the same internal circuitry as semiconductor integrated circuit 50. Therefore, components and component numbers described in semiconductor integrated circuit 50 are herein discussed as being in any of the semiconductor integrated circuits 115-117 of the invention. The load board interface 75 has four sets of pins 122-125 for connection to I/O pins 70 and 1/0 pins 126-128 of semiconductor integrated circuits 50 and 115-117, respectively. Each group of pins 122-125 are connected internally on the load board interface 75 to load board pins 130, which in turn are connected to pins 120. Thus, the test station 60 has the ability to apply input test signals to semiconductor integrated circuits 50 and 115-117 when connected to the circuits through the load board interface 75. Internal circuitry on load board interface 75 responds to the output enable signal to switch the internal connections of pins 123-D, 124-D and 125-D from pin 130-D to pins 130-C, 130-B, and 130-A, respectively, in order to supply a compressed test output signal from each of

the semiconductor integrated circuits 50 and 115-117 to one test station, in this case test station 60, during the first test mode. Thus, the semiconductor integrated circuit and load board interface of the invention allow one test station to simultaneously perform the circuit tests on four semiconductor integrated circuits rather than one.

[0017] Thus, during testing in the first test mode of the semiconductor integrated circuit 50, the test station I/O pin 120-D receives a compressed test output signal from I/O pin 70-D through internal circuitry of the load board interface 75. Similarly, pins 120-A,B and C receive compressed test output signals from I/O pins 128-D, 127-D, and 126-D respectively. The circuitry of test station 60 determines from the potential or impedance on pin 120 whether the semiconductor integrated circuits 50 and 115-117 meet circuit test requirements. When the potential has a high or low logic state, the semiconductor integrated circuit meets the circuit test requirements of the first test mode. When a pin 120 is held at a high impedance, at least one of the circuit functions creating the output test data at nodes 95 of the pertinent semiconductor integrated circuit 50 or 115-117 does not meet circuit test requirements of the first test mode.

[0018] Although device input and output nodes have been referred to as input “pins” and output “pins”, the gender of the “pins” is not necessarily male and may very well be female. Typically, the “pins” of the semiconductor integrated circuit of the invention and the load board interface of the invention and the test station are made in order to couple two devices with a male/female connection.

[0019] In the case where at least one of the semiconductor integrated circuits does not meet at least one circuit test requirement of the first test mode, a second test mode can be enabled to determine which circuit test is failing. During the second test mode, all four I/O pins 70, 126, 127 or 128 of the faulty device are connected to pins 122A-D. The test mode signal switches state to a second logic state to disable comparator circuit 100 and enable the buffer enable bank 105 for the second test mode, thereby allowing the test data outputs at nodes 95 to be driven to the I/O pins 70, 126, 127, or 128 through the buffer enable bank 105 and the input/output buffer 80. Now the test station 60 of the memory component tester can determine which of the four tests, represented by the test data now driven to pins 120 by the load board interface 75, do not meet circuit requirements.

[0020] During normal operation, the buffer enable bank 105 is disabled for the first test mode and enabled for normal operation by the test mode signal having the second logic state at node 118 in order that user data can be driven from nodes 95 through the buffer enable bank 105 and the input/output buffer 80 to 110 pins 70, 126, 127, or 128.

[0021] The circuitry of the semiconductor integrated circuit of the invention, which compresses four test output signals to provide one test output signal in a first test mode, and the load board interface of the invention facilitate a reduction in hardware requirements during test and decrease test time. The hardware reduction is realized by the connection and testing of four semiconductor integrated circuits with one station rather than four test stations.

[0022] Although the semiconductor integrated circuits 50, 115-117 and load board interface 75 and test station 60 have been shown having groups of four I/O pins, the semiconductor integrated circuit and load board interface of the invention have applicability in cases where the number of I/O pins is greater or less than four. Thus, with an advent of more I/O pins, the number of semiconductor integrated circuits that can be simultaneously tested by one test station can be increased as long as the test station has a corresponding increase in I/Os.

[0023] Although the invention has been shown wherein a corresponding I/O pin D (70-D, 126-D, 127-D, and 128-D) on all of the semiconductor integrated circuits 50 and 115-117 is connected to an input pin 120 of test station 60 through load board interface 75, any one of the I/O pins 70 and 126-128 A-D may be selected for connection by altering the load board interface circuitry in order to multiplex the I/O pins 70 and 126-128 differently to test station 60 during the analysis of the compressed test output signals. Typically, this would occur in a case where the internal circuitry of the semiconductor integrated circuit of the invention is modified in order for the compressed output signal to appear at an I/O other than D.

[0024] Other variations include load board interface circuitry having two (or some other number) sets, rather than four sets of I/O pins 122-125, for connection to two semiconductor integrated circuits of the invention rather than four.

[0025] Figure 3 is a simplified block schematic of one load board interface 75. Pins 123-D, 124-D, and 125-D are connected to switching circuits 133, 134, and 135 respectively. When the load board interface is connected to the test station 60 of Figure 2, the switching

circuits 133, 134 and 135 connect pin 130-D to pins 123-D, 124-D, and 125-D, respectively, when the test station 60 is supplying test input data to the semiconductor integrated circuits 50 and 115-117 of Figure 2; and the switching circuits 133, 134, and 135 connect pins 123-D, 124-D, and 125-D to pins 130-C, 130-B, and 130-A, respectively, when the test station 60 is receiving compressed test output signals from each of the semiconductor integrated circuits 50 and 115-117. The switching circuits switch between the two connections in response to the output enable signal at node 76.

[0026] Figure 4 is a schematic of the buffer enable bank 105. The circuitry in each block A-D is shown. It can be seen by studying the schematic that output nodes 119 have a high impedance when the test mode enable signal at node 118 is high, thereby disabling the buffer enable bank 105 during the first, test mode. When the test mode enable signal is low, the test mode buffer enable bank 105 is enabled for the second test mode and for normal circuit operation. During the second test mode and during normal operation, the test output data or user data on nodes 95 is driven through the buffer enable bank 105 to nodes 119 and then through input/output buffer 80 to input/output pins 70 (see Figure 2). The low test mode signal also disables the comparator circuit 100 during the second test mode or during normal operation. It is possible within the spirit and scope of the invention to use other circuitries to perform the function of the buffer enable bank 105.

[0027] Figure 5 is the comparator circuit 100 of the semiconductor integrated circuit 50 of the invention. The test mode enable signal having the first logic state enables AND gate 210 and negative AND gate 215. When the output test data on all of the nodes 95 have a high logic state, the output of AND gate 210 is high which actuates NMOS transistor 220 driving comparator output node 110 to a potential having a high logic state indicating that the semiconductor integrated circuit passes the circuit tests. When the output test data on all of the nodes 95 have a low logic state, the output of negative AND gate 215 is high which actuates NMOS transistor 225, driving the potential of comparator output node 110 to a potential having a low logic state indicating that the semiconductor circuit passes the circuit test. When the potentials on nodes 95 have different logic states, the outputs of AND gate 210 and negative AND gate 215 are low and transistors 220 and 225 are deactuated. In this case, comparator

output node 110 has a high impedance indicating that at least one of the data signals on nodes 95 is not correct. Thus, the comparator circuit 100 compresses the four output test data on nodes 95 into one test output signal at node 110. It is possible for other circuit implementations to replace the implementation shown in Figure 5 without departing from the spirit and scope of the invention.